

LS XGK Cnet

Supported Series: LS XGT series XGK CPU with communication module XGL-CH2A

Website: <http://www.lgjs.com/>

HMI Setting:

Parameters	Recommended	Options	Notes
PLC type	LS XGK Cnet		
PLC I/F	RS232	RS232/RS485 4W	
Baud rate	115200	9600~115200	
Data bits	8	7, 8	
Parity	None	Even, Odd, None	
Stop bits	1	1	
PLC sta. no.	1	0 ~ 32	

Online simulator	YES	Pass-Through	YES
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Device Address:

Bit/Word	Device type	Format	Range	Memo
B	PW_Bit	DDDDh	0 ~ 4095f	I/O device Bit
B	MW_Bit	DDDDh	0 ~ 4095f	Internal device Bit
B	LW_Bit	DDDDDh	0 ~ 11263f	Communication device Bit
B	KW_Bit	DDDDh	0 ~ 4095f	Preservation device Bit
B	FW_Bit	DDDDh	0 ~ 4095f	Special device Bit(write available from 1025)
B	DW_Bit	DDDDDDh	0 ~ 524287f	Data register_Bit expression (D0000.0)
B	UW_Bit	DH.DDh	0 ~ 7f.31f	XGK-CPUE : hh(0~1f)
B	RW_Bit	DDDDDDh	0 ~ 32767f	
B	ZRW_Bit	DDDDDDh	0 ~ 32767f	
B	NW_Bit	DDDDDDh	0 ~ 21503f	
B	ZW_Bit	DDDDh	0 ~ 255f	
B	SX	DDDDD	0 ~ 25599	Relay for step control Bit
B	TX	DDDD	0 ~ 8191	Timer device Bit
B	CX	DDDD	0 ~ 4095	Counter device Bit
W	PW	DDDD	0 ~ 4095	I/O device
W	MW	DDDD	0 ~ 4095	Internal device

Bit/Word	Device type	Format	Range	Memo
W	LW	DDDDD	0 ~ 11263	Communication device
W	KW	DDDD	0 ~ 4095	Preservation device
W	FW	DDDD	0 ~ 4095	Special device(write available from 1025)
W	DW	DDDDDD	0 ~ 524287	Data register
W	UW	DH.DD	0.00 ~ 7f.31	Analog data register XGK-CPUE : hh(0~1f)
W	RW	DDDDD	0 ~ 32767	
W	ZRW	DDDDD	0 ~ 32767	
W	NW	DDDDD	0 ~ 21503	Communication data register
W	ZW	DDD	0 ~ 255	Index register_128 words
W	SW	DDDDD	0 ~ 255	Relay for step control
W	TW	DDDD	0 ~ 8191	Timer current value register
W	CW	DDDD	0 ~ 4095	Counter current value register

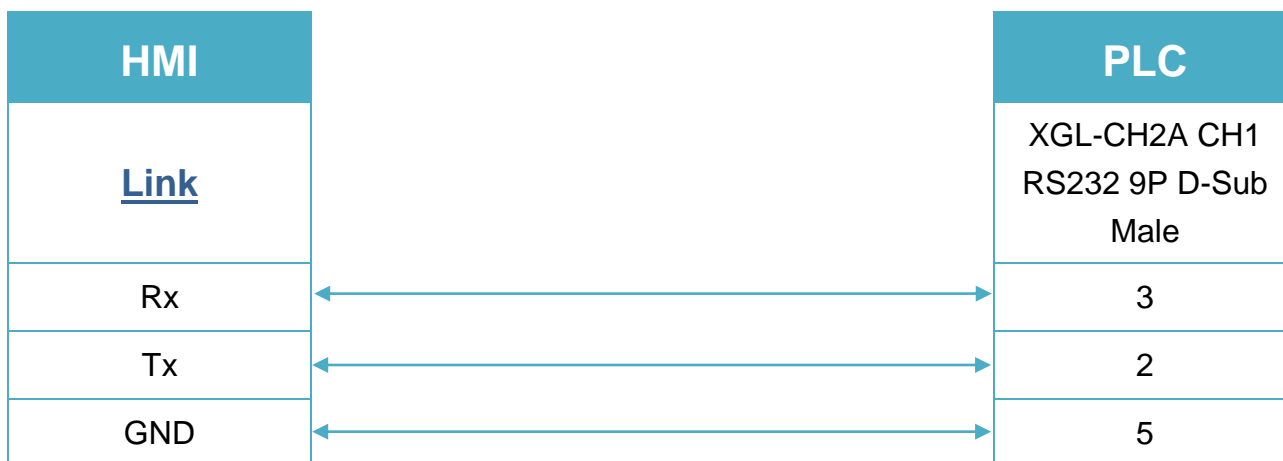
Wiring Diagram:

XGL-CH2A CH1 RS232 9P D-Sub Male

Diagram 1

RS-232

The serial port pin assignments may vary between HMI models, please click the following link for more information.



XGL-CH2A CH2 5P Terminal

Diagram 2

RS-485 4W

The serial port pin assignments may vary between HMI models, please click the following link for more information.

